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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/758,205	01/16/2004	Hideki Higashitani	2004-0067	4879

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EXAMINER	
LAM, CATHY FONG FONG	
ART UNIT	**PAPER NUMBER**
1775	

DATE MAILED: 09/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/758,205	HIGASHITANI, HIDEKI	
	Examiner	Art Unit	
	Cathy Lam	1775	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-18* is/are allowed.

6)☒ Claim(s) *19-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/420,876.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date ____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

In view of the amendment and remarks filed on June 30, 2006, applicant has amended the specification to include 10/420,876 as continuation data of the present application. Applicant is suggested to also include 10/758,204 and 10/758,129 (and their current status) as related application, to be part of the continuation data.

Claims 15-28 are currently pending in the application, claims 19-28 are unpatentable as following:

Claim Rejections - 35 USC § 112

1. Claims 25 and dependents are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 25, it is vague and indefinite as to which of the electrically insulating substrates is the component embedded within?

Claim 26 is structurally indefinite.

Claim 27 is indefinite, as there is no antecedent basis for "wiring layers arranged on.....second electrically insulating substrate". Clarification is required.

Claim Rejections - 35 USC § 103

1. Claims 19-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andou et al (US 6197407) or Chen et al (US 6346335) or Hayashi (US 6359235) in view of Chen (US 5250363).

Applicant is reminded that it is the product itself which must be new and unobvious, see In re Pinkington 162 USPQ 145, 147 (C.C.P.A. 1969). Product by

process claimed are not patentably distinct over product claims unless it can be shown that the product produced by the process is in some manner measurably distinct from the product produced by another process, therefore there will be no weight given to the product by process verses product claims.

Andou teaches a circuit board comprised of an electrical insulating substrate, an adhesive and a wiring transfer layer (Fig. 1(f)).

Adhesive layers (101) are formed over the electrical insulating substrate (102). The adhesive layers are semi-cured thermosetting resin (col 3 L 24-27 & L 34-35). Through holes are formed in the electrical insulating substrate, and conductive paste is filled into the through holes (col 3 L 3-6).

A wiring transfer layer comprised of a supporting base (106) and wiring layers (107) are superposed onto both surfaces of the electrically insulating substrate and over the filled through holes (col 9 L 66-col 10 L 5).

Since the adhesive layers on the insulating substrate are uncured layers, when the wiring transfer layers bring into contact with the adhesive layers, the adhesive layers would conform to any surface roughness (or condition) of the wiring transfer layer. The examiner takes the position that the adhesive layers (101) are part of the electrical insulating substrate (102).

Andou also teaches a multilayer circuit board by stacking a plurality of single circuit board (col 15 L 9-34 & Figs. 4(a) –(e)).

Chen '335 discloses a composite material comprised of a support layer (12), a copper foil (14) and a bond strength enhancing agent (20).

The copper foil (14) is releasably formed onto the support layer (12) and the bonding strength enhancing agent (20) is formed onto the surface of the copper foil that faces away from the support layer (Fig. 1). The bond strength enhancing agent (20) are copper dendrites (col 4 L 49-53).

The composite is bonded to a dielectric substrate (22) which may be a rigid or a flexible layer. An adhesive may be used for bonding between a rigid dielectric substrate and the composite. For a flexible board, the dielectric substrate is an uncured liquid or gel polymer cast onto the composite foil (col 5 L 1-20).

The examiner takes the position that the dielectric substrate has a surface that conforms to the surface of the copper foil (14), or the dielectric surface is complementary to the copper foil surface.

Hayashi discloses a multilayer wiring board having an electronic device (or a component) embedded.

The multilayer wiring board is comprised of a plurality of single wiring boards. The single wiring board is comprised of a semi-cured insulation sheet (1) and a wiring transfer film (5). A wiring pattern (4) is formed onto the wiring transfer film (5). The insulating sheet (1) has through holes (2) formed in the thickness direction and conductive paste (3) is filled into the through holes (2). The wiring transfer film (5) is brought into contact with the insulating sheet (1) and the wiring pattern is bonded to the surface of the insulating sheet (1) and in electrical contact with the conductive paste (3) (col 5 L 35-38 & L 57-58), Figs. 1A-1E).

The examiner takes the position that the insulating sheet conforms the shape of the wiring pattern of the transfer film, in other words the uncured insulating sheet is complementary to the surface of the wiring transfer film.

A semiconductor device (or a component) is embedded within the multilayer wiring board (Figs. 6A-6E & col 9 L 28-35).

Andou, Chen '335, and Hayashi teach a printed wiring board comprised of a wiring transfer sheet and an insulating substrate. The wiring transfer sheet has a wiring pattern formed on its surface that bring into contact with a semi-cured surface of the insulating substrate.

The examiner takes the position that the insulating substrate has the surface complementary to the surface of the wiring transfer sheet.

The prior art however do not teach the surface of the insulating substrate has a plurality of convexities nor the surface of the transfer sheet has a plurality of concavities.

Chen '363 teaches a printed circuit board comprised of a conductive foil and a dielectric substrate. The conductive foil has a roughened surface that would be bonded to the dielectric substrate (32) (col 1 L 51-53).

The roughened surface is made from a plurality of dendrites on *at least* a first surface (or the bonding surface). The dendrites are usually formed by electrolytic deposition (col 5 L 15-18).

In view of the Figures, the dielectric substrate (32) has its bonding surface conforms to the surface roughness of the conductive foil (12) (Fig. 3). The examiner

takes the position that the dielectric substrate has a plurality of convexities and the conductive foil has a plurality of concavities on its bonding surface.

The examiner also takes the position that Andou, Chen '335 and Hayashi all have a surface roughness that conforms to the wiring transfer layer or the wiring support layer. Since applicant has not claimed any surface roughness nor dimensions of the convexities and/or concavities, all the cited prior art *inherently* possess a surface roughness that microscopically has convexities and concavities.

Regarding to the dielectric substrate has convexities occupy 50-98% of the exposed area. The examiner takes the position that convexities and concavities can easily be made by pressing a layer with surface concavities and convexities, respectively, to reach the desired volume %. Furthermore, it is conventional to roughen a surface by electrolytically depositing dendrites on the surface of a metal layer.

Allowable Subject Matter

2. Claims 15-18 are allowed.

3. Claim 19 and its dependents would be allowable if rewritten to incorporate the diameter and the height of the convexities limitations as described in claim 18.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cathy Lam whose telephone number is (571) 272-1538. The examiner can normally be reached on 9am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jennifer McNeil can be reached on (571) 272-1540. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cathy Lam

Cathy Lam
Primary Examiner
Art Unit 1775

cfl
September 05, 2006